IN THE CLAIMS:

Claim 1 has been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A memory device, comprising:

a memory array for storing at least one data bit and configured to electrically operate from a power supply voltage; and

a circuit configured to receive an external reference voltage as generated external to the memory device and generate in response thereto an internal reference voltage independent of the power supply voltage, the internal reference voltage for accessing and evaluating a logic state of the at least one data bit in the memory array.

2. (Previously Presented) The memory device of claim 1, further comprising data input/output circuitry coupled to the memory array and further coupled and responsive to the internal reference voltage of the circuit.

3. (Previously Presented) The memory device of claim 1, further comprising an address register coupled and responsive to the internal reference voltage of the circuit.

4. (Previously Presented) The memory device of claim 1, wherein the internal reference voltage generated by the circuit tracks follows the external reference voltage.

5. (Previously Presented) The memory device of claim 1, wherein the circuit comprises a following circuit configured to generate an internal reference voltage that is dependent upon the external reference voltage.

6. (Previously Presented) The memory device of claim 1, wherein the circuit comprises a voltage follower configured to receive the external reference voltage at an input and to generate in response thereto the internal reference voltage.

7. (Previously Presented) The memory device of claim 1, wherein the circuit comprises a plurality of voltage followers serially coupled to receive the external reference voltage and generate in response thereto the internal reference voltage.

8. (Previously Presented) The memory device of claim 1, further comprising circuitry for configuring the memory device as one of a DRAM, SDRAM, Rambus memory, double data rate memory and flash memory.